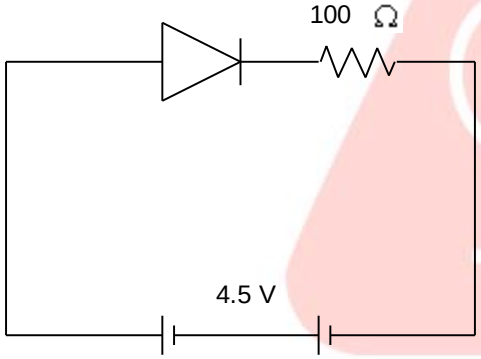
DPP
DAILY PRACTICE PROBLEMS

Class : XIIth **Subject : PHYSICS**
Date : **DPP No. : 2**

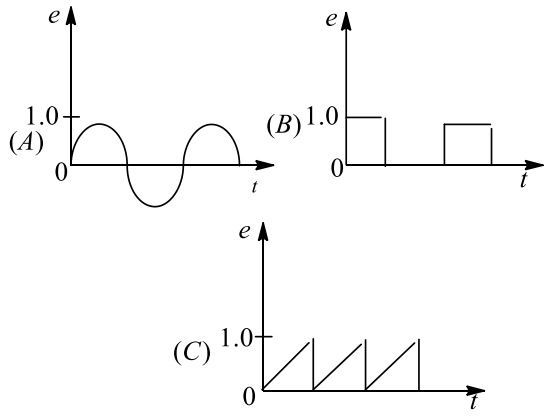
Topic :-.SEMICONDUCTOR ELECTRONICS: MATERIALS,DEVIES AND SIMPLE CIRCUITS

1. Which of the following is not equal to 1 in Boolean algebra?
   a) $\overline{A \cdot \overline{A}}$ b) $A \cdot \overline{A}$ c) $A + \overline{A}$ d) $A + 1$
2. The electrical conductivity of an intrinsic semiconductor at 0 K is
   a) Less than that of an insulator b) Is equal to zero
   c) Is equal to infinity d) More than that of an insulator
3. Figure shows a diode connected to an external resistance and an emf. Assuming that the barrier potential developed in diode is 0.5 V, obtain the value of current in the circuit in milli ampere.



   a) 40 mA b) 60 mA c) 80 mA d) 100 mA
4. Based on the energy band description, a solid can be classified as a semiconductor if the energy gap between the valence band and conduction band is
   a) $3eV < E_g < 6\ eV$ b) $E_g > 6\ eV$ c) $E_g < 3\ eV$ d) $E_g = 0eV$
5. If the ends p and n of $p-n$ diode junction are joined by a wire
   a) There will not be a steady current in the circuit
   b) There will be a steady current from n-side to p-side
   c) There will be a steady current from p-side to n-side
   d) There will not be a current depending upon the resistance of the connecting wire
6. Which of the following materials in non crystalline
   a) Copper b) Sodium chloride c) Wood d) Diamond
7. The correct relation between n_e and n_h in an intrinsic semiconductor at ordinary temperature is
   a) $n_e > n_h$ b) $n_e < n_h$ c) $n_e = n_h$ d) $n_e = n_h = 0$

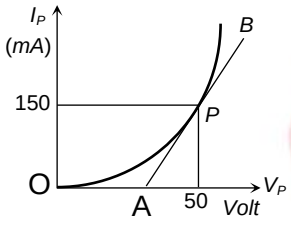
8. The time variations of signals are given as in A, B and C. Point out the true statement from the following.



a) A, B and C are analogue signals
b) A and B are analogue, but C is digital signal
c) A and C digital, but B is analogue signal
d) A and C are analogue but B is digital signal

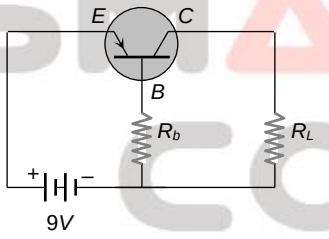
9. The reverse biasing in a PN junction diode
a) Decreases the potential barrier
b) Increases the potential barrier
c) Increases the number of minority charge carriers
d) Increases the number of majority charge carriers

10. The plate characteristic curve of a diode in space charge limited region is as shown in the figure. The slope of curve at point P is 5.0 mA/V. The static plate resistance of diode will be



a) 111.1Ω b) 222.2Ω c) 333.3Ω d) 444.4Ω

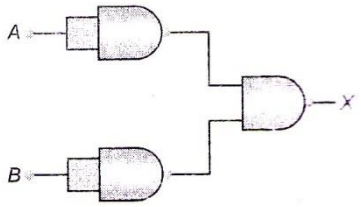
11. In a transistor circuit shown here the base current is 35 μA. The value of the resistor R_b is



a) 123.5 $k\Omega$ b) 257 $k\Omega$ c) 380.05 $k\Omega$ d) None of these

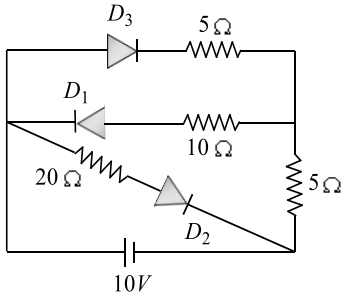
12. When forward bias is applied to a P-N junction, then what happens to the potential barrier V_B, and the width of charge depleted region x
a) V_B increases, x decreases
b) V_B decreases, x increases
c) V_B increases, x increases
d) V_B decreases, x decreases

13. The combination of gates shown below yields



a) OR gate b) NOT gate c) XOR gate d) NAND gate

14. In the given circuit



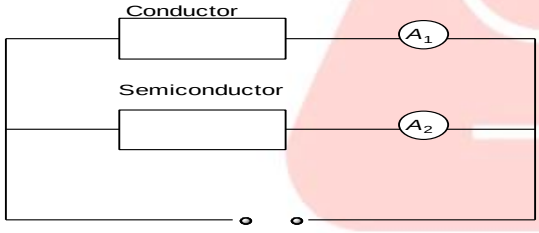
The current through the battery is

a) 0.5 A b) 1 A c) 1.5 A d) 2 A

15. To obtain electrons as majority charge carriers in a semiconductor, the impurity mixed is

a) Monovalent b) Divalent c) Trivalent d) Pentavalent

16. A conductor and a semiconductor are connected in parallel as shown in the figure. At a certain voltage both ammeters register the same current. If the voltage of the DC source is increased then the



a) Ammeter connected to the semiconductor will register higher current than the ammeter connected to the conductor

b) Ammeter connected to the conductor will register higher current than the ammeter connected to the semiconductor

c) Ammeters connected to both semiconductor and conductor will register the same current

d) Ammeters connected to both semiconductor and conductor will register no change in the current

17. Platinum and silicon are heated upto 250°C and after that cooled. In the process of cooling

a) Resistance of platinum will increase and that of silicon will decrease

b) Resistance of silicon will increase and that of platinum will decrease

c) Resistance of both will increase

d) Resistance of both will decrease

18. Consider the following statements *A* and *B* and identify the correct choice of the given answers

A. The width of the depletion layer in a *P*-*N* junction diode increases in forward bias

B. In an intrinsic semiconductor the fermi energy level is exactly in the middle of the forbidden gap

a) *A* is true and *B* is false b) Both *A* and *B* are false

c) *A* is false and *B* is true d) Both *A* and *B* are true

19. The symbolic representation of four logic gates are given below

(i) 

(ii) 

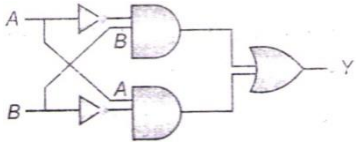
(iii) 

(iv) 

The logic symbols for OR, NOT and NAND gates are respectively

a) (iii), (iv), (ii) b) (iv), (i), (iii) c) (iv), (ii), (i) d) (i), (iii), (iv)

20. The truth table for the following logic circuit is



a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

b)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

c)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

d)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1